Static Timing Analysis:

Timing Path:

Identifying the timing path is the first and the most important thing to do in static timing analysis. A timing path will have a start point and an end point. The start point is either a Flop clk pin or input ports and the end point is either a Flop d pin or output ports. Below is the figure showing all 4 combinations of the timing paths.

Diagram

Description automatically generated

Arrival Time

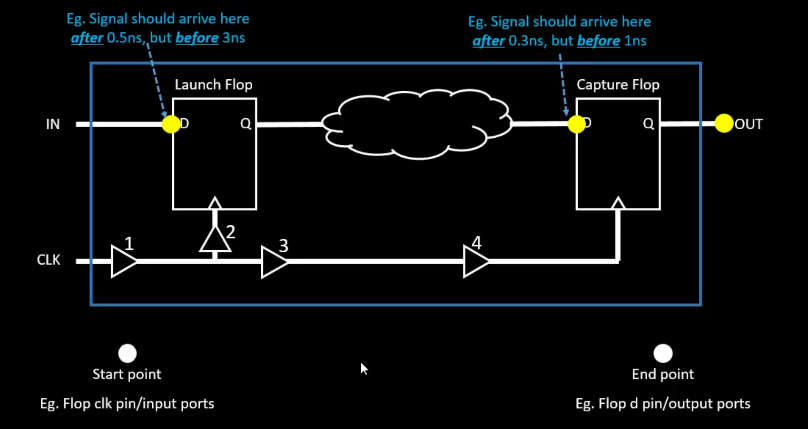
The time required for a signal to reach the end point from the start point is called arrival time. It is calculated at the end points. When there are more than one timing paths for one end point then calculating the arrival point becomes tricky.

Text

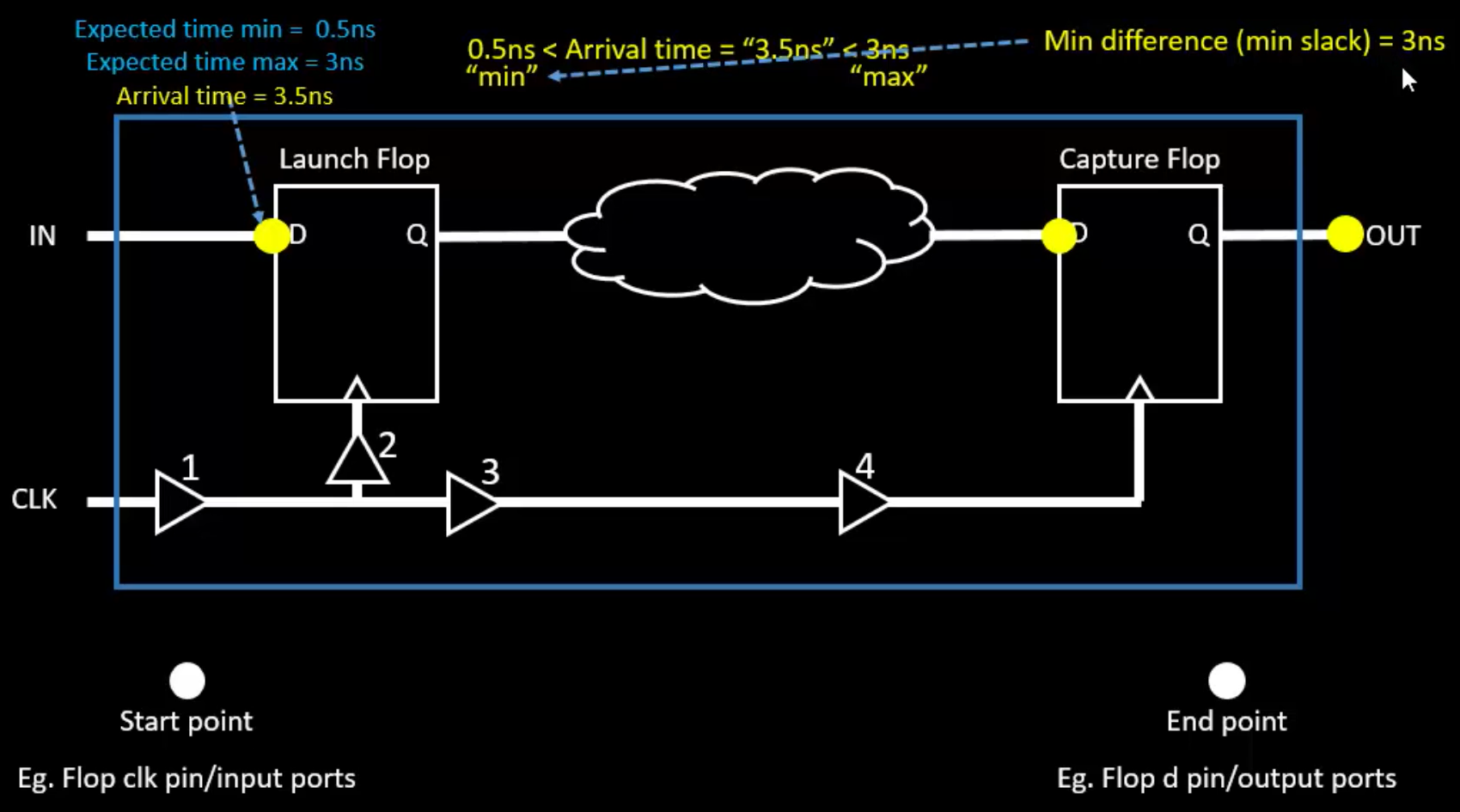
Description automatically generated

Required Time

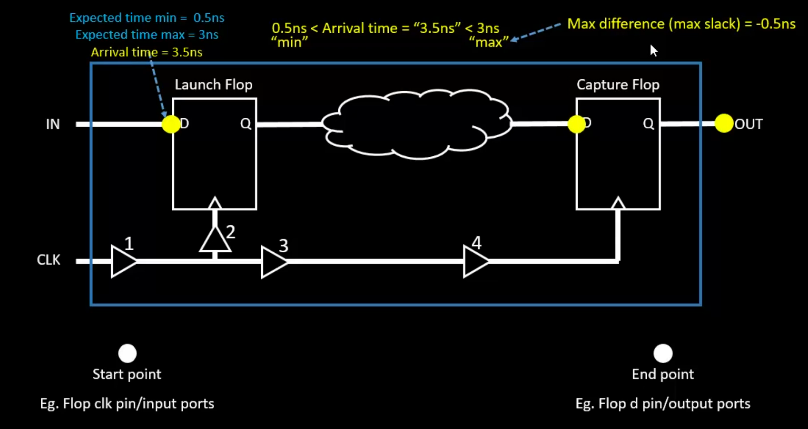
Required time defines the needs of the system or the specifications of the system. In other words, it is the expected time for the signal to arrive. These values are specified by the constraints. In the below example, if we consider that the signal should arrive after 0.5 ns and before 3ns, it implies that the arrival time should lie between 0.5 and 3 ns. Hence 0.5 ns can be considered as the minimum expected time and 3 ns can be considered as the maximum expected time. Also, let us suppose that the arrival time is 3.5ns. In this case, it satisfies one of the conditions and does not satisfy the other.

  
Slack

Slack is the difference between the arrival time and the required (expected time). Consider the below example,



Min difference or min slack = Arrival time - expected time = 3.5 - 0.5 ns = 3ns. Also referred to as hold slack or hold timing or hold analysis.

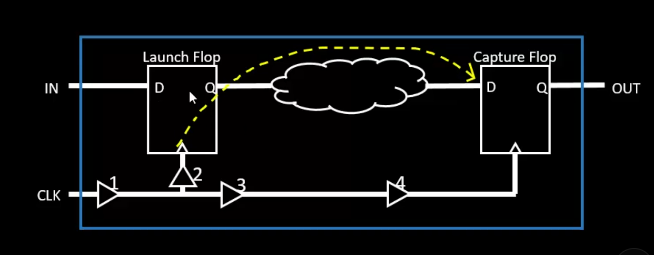


Max difference or max slack = Required time - arrival time = 3 - 3.5 = -0.5 ns --> This means that the signal is delayed by 0.5 ns and it needs to be taken care of. Also referred to as setup slack or setup timing or setup analysis

**Types of Setup/ Hold analysis**

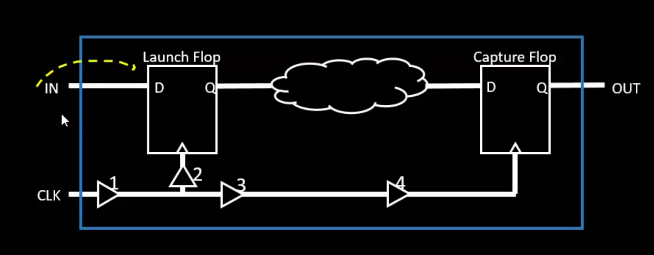
1. **reg2reg**

Any path crossing from a register to register. In the below example, the path is from a launch flop to a capture flop



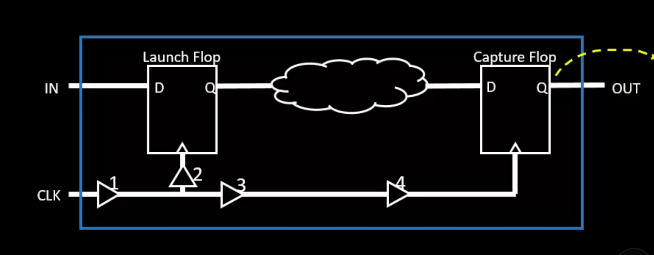
1. **in2reg**

Timing path between input port (not the clock ports) to D pin of the launch flop



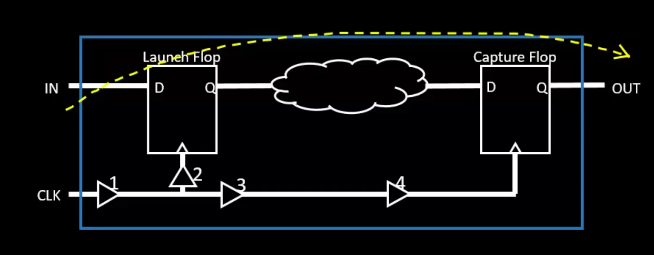
1. **reg2out**

Timing path from capture flop output to output port



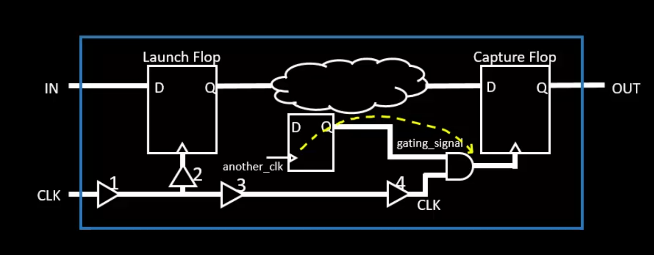
1. **in2out**

Timing path from input port to output port



There are many more categories for analysis. To understand the other categories, we finetune the circuit to include clock gating. the capture flop is not given the clock directly but through another circuit. The clock gating technique is widely used to reduce the amount of chip power.

1. **Clock Gating**

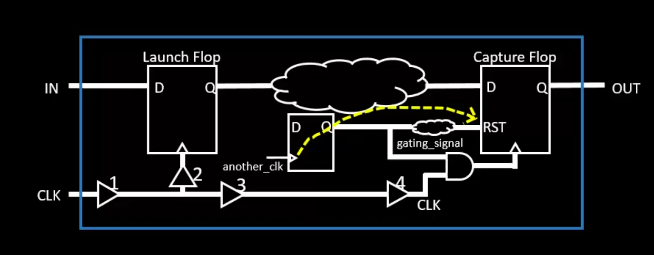


As there is a new clock, there is a new timing path. Whenever the gating\_signal is high, clock is given to the capture flop and when the gating\_signal is 0, clock is not supplied to the capture flop. This now involves a new category of analysis, known as clock gating analysis for the path between the new clock and the AND gate output

1. **Recovery/ removal**

Considering asynchronous pins of the flop, for example, reset.

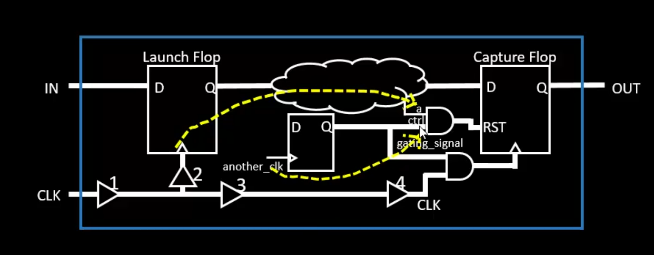
Recovery/ removal timing analysis involves the timing path is between the new clock and the reset pin. The reset signal should arrive after a particular time after the clock signal.



1. data-to-data

To save some amount of power in the reset path, the circuit is modified as below. A control signal is introduced to control the gating signal. Based on the A and control signal, the capture flop might be set or reset and hence some leakage power can be saved accordingly.

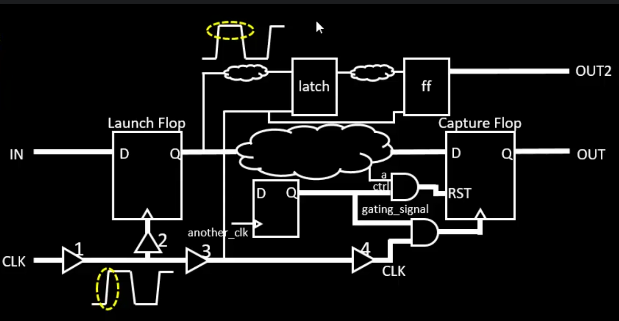
The specification is that the A and control signal should be in sync. The A and the control pin should be treated as end points. Then we get different timing paths corresponding to that, as shown below. These timing paths need a data check analysis. A timing path between 2 data signals is considered as data-to-data analysis.



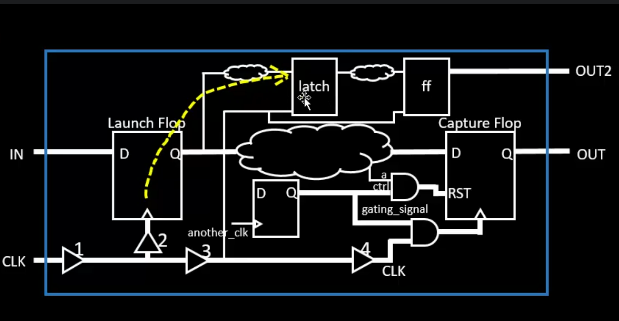
The requirement could be that the A signal should arrive later than control signal and this can be ensured with this kind of timing analysis. Few constraints could be applied to meet this requirement.

1. **Latch (time borrow/ time given)**

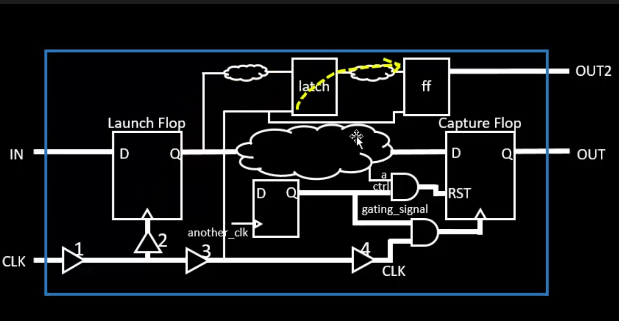
Launch flop becomes transparent at the edge of the clock signal. Latch becomes transparent at the level of the clock pulse.



If the timing path constraint from the flop to latch is not met, the flop can borrow some time from the area of level of the clock signal.



If the timing path constraint from the latch to the flop is not being met, some time can be given from the level of clock signal area to the start point i.e. the flop.



We also have the slew/ transition analysis, which have to met i.e., should be in between a particular min or max value.